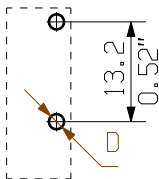
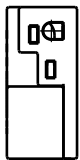
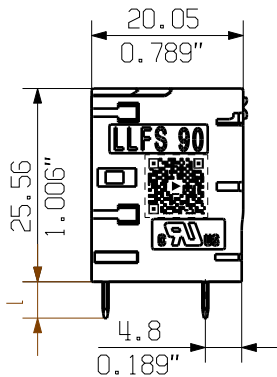
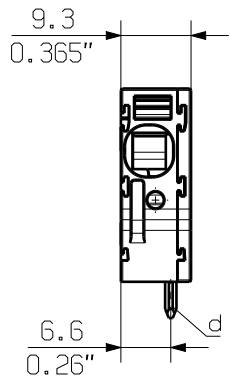


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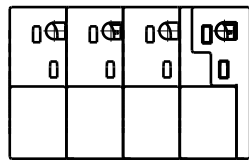
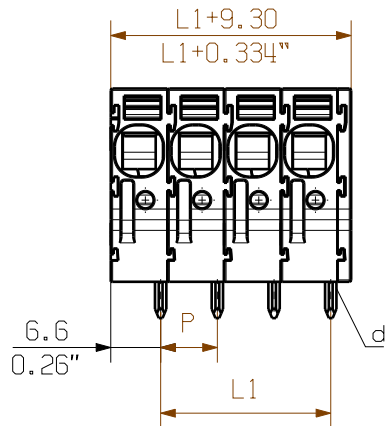
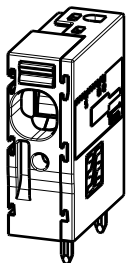
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General customer drawing, topical version only if required

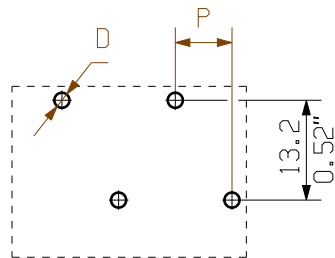
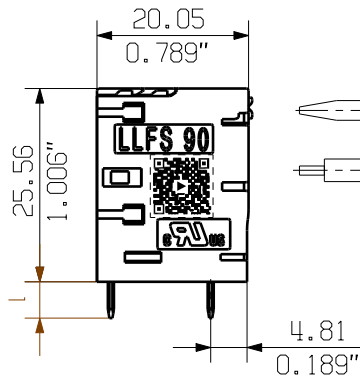
The English version is binding



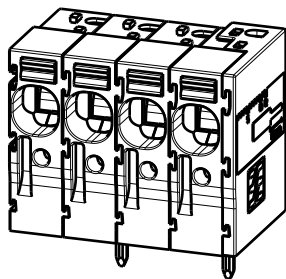
Hole pattern



Pole: 1 2 3 4...



Hole pattern



P = 7.50
0.295" (Pitch)
D = Ø2 +0.1
0.079"
d = 1.5x0.8
0.059"x0.031"
l = 5.0 +0.2 -0.6
0.197"

12	82.50	3.248
11	75.00	2.953
10	67.50	2.657
9	60.00	2.362
8	52.50	2.067
7	45.00	1.772
6	37.50	1.476
5	30.00	1.181
4	22.50	0.886
3	15.00	0.591
2	7.50	0.295
n Poles	L1 [mm]	L1 [inch]

For the mounting of PCBs, it should be noted that the rated data relates only to the PCB components alone. The necessary creepage and clearance paths must be observed in connection with the respective applicant in accordance to IEC 60664-1 (VDE 0110). The current-carrying capacity and pitch tolerance is to be determined according to DIN IEC 60326-3 very fine.

Weidmüller PCB components are tested to the IEC 60947-7-4 standard, and are valid for its field of application. Provided that the components are used to the intended purpose, all requirements with respect to the occurring of electrical, mechanical, thermic and corrosive stress will be satisfied.



General Tolerances: <input type="checkbox"/> WN700144-W.. <input type="checkbox"/> WN 212010 <input checked="" type="checkbox"/> ISO 2768-mK		Tolerances ISO 8015	
Changes: EC00005454 1		Weidmüller	
Mat. No. (SAP) 2473020000			
Drawings Assembly		61340 10 Drawing no. Index Scale: 2:1 Sheet 2 / 4	
Drawn	Xiang, Keqin		
Responsible	Xiang, Keqin		
Approved	Xu, Shary	18.01.2022	
		LLFS 7.50/.../90 ... PCB TERMINAL LEITERPLATTENKLEMME	